**Lab manual Q.no 9)**

**1)Understanding the Problem:**

In the above program we need to implement a 4to1 mux using 32 bit inputs.A mux selects one of the data ips given to it depending on the select line & connects it to op.Here we have to use a Bus as it is a Multi bit ip.

**2) Devising a Plan/Design:**

In this program we need to just use conditional operator(?:) to execute the design.We may use any type of modeling. In this if select line is 0 output is D0. select line is 1 output is D1 so on.The truth table is as shown:

|  |  |  |
| --- | --- | --- |
| s1 | s0 | output |
| 0 | 0 | D0 |
| 0 | 1 | D1 |
| 1 | 0 | D2 |
| 1 | 1 | D3 |

Here the ip is a bus of 32 bit size.

**3) Carrying out the plan:**

**Verilog code:**

module thirtytwo\_mux(

input s1,

input s0,

input [31:0] D3,

input [31:0] D2,

input [31:0] D1,

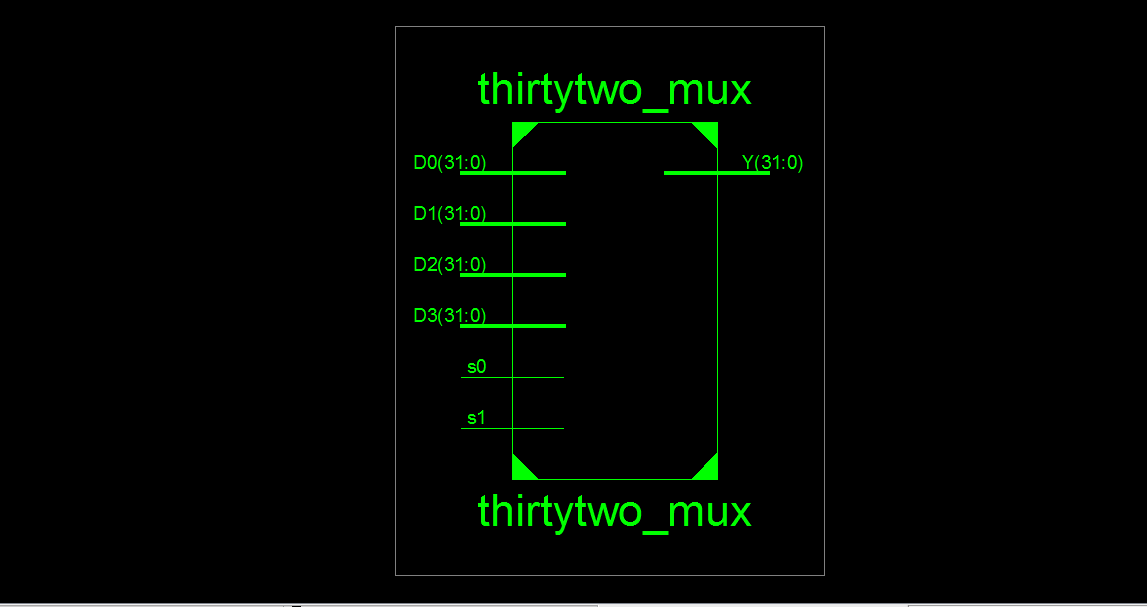
input [31:0] D0,

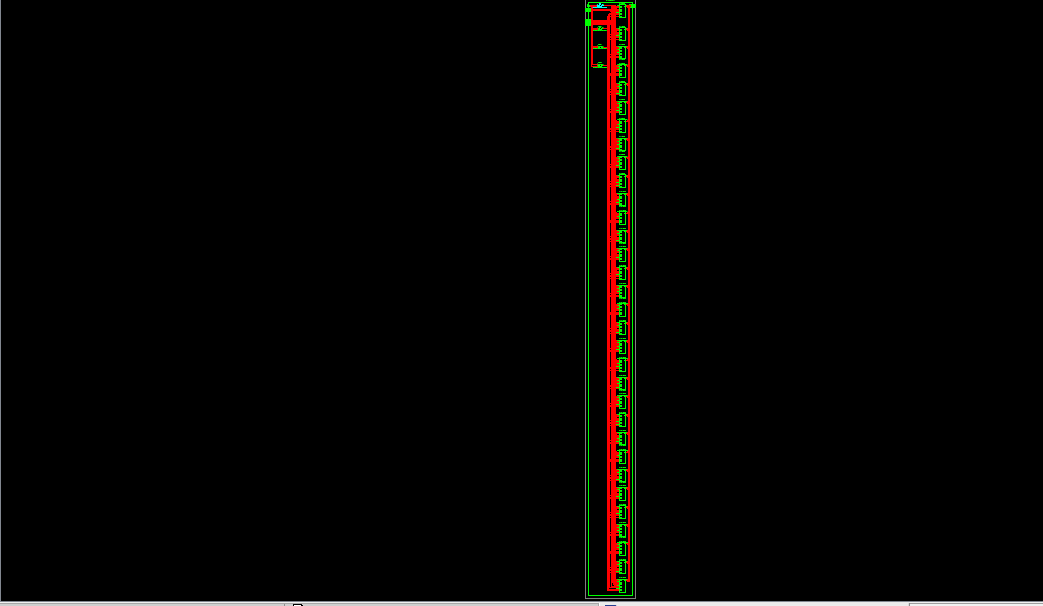
output [31:0] Y

);

assign Y=(s1==1'b1&s0==1'b1)?(D3):((s1==1'b1&s0==1'b0)?(D2):((s1==1'b0&s0==1'b1)?(D1):((s1==1'b0&s0==1'b0)?(D0):1'b0)));

endmodule





**Testbench:**

module thirtytwo\_mux\_tb;

// Inputs

reg s1;

reg s0;

reg [31:0] D3;

reg [31:0] D2;

reg [31:0] D1;

reg [31:0] D0;

// Outputs

wire [31:0] Y;

// Instantiate the Unit Under Test (UUT)

thirtytwo\_mux uut (

.s1(s1),

.s0(s0),

.D3(D3),

.D2(D2),

.D1(D1),

.D0(D0),

.Y(Y)

);

initial begin

// Initialize Inputs

s1 = 0;

s0 = 0;

D3 = 0;

D2 = 0;

D1 = 0;

D0 = 0;

// Wait 100 ns for global reset to finish

#100;

// Add stimulus here

s1=1'b1;

s0=1'b1;

D3=32'b11001100110011001001100110011001;

D2=32'b11111111111111111111111111111111;

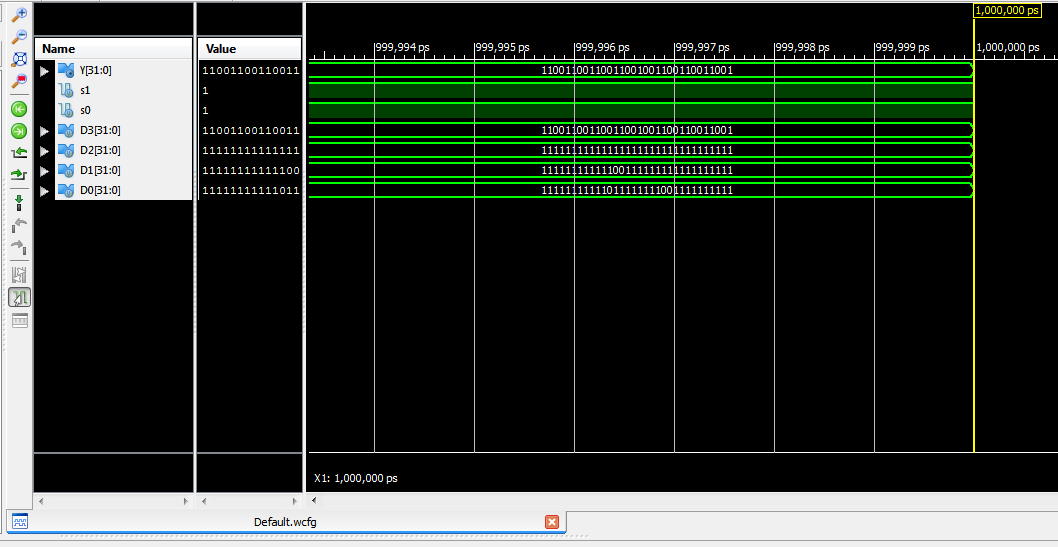
D1=32'b11111111111100111111111111111111;

D0=32'b11111111111011111111001111111111;

#100;

end

endmodule



**4)Looking back/Self reflection:**

In this program we have seen the implementation of a 4to1 MUX with ips of 32 bits each.The hardware required for the implementation is more.So sometimes the hardware gets overloaded.

***Synthesis report:***

Release 12.1 - xst M.53d (nt)

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--> Parameter TMPDIR set to xst/projnav.tmp

Total REAL time to Xst completion: 0.00 secs

Total CPU time to Xst completion: 0.39 secs

--> Parameter xsthdpdir set to xst

Total REAL time to Xst completion: 0.00 secs

Total CPU time to Xst completion: 0.41 secs

--> Reading design: thirtytwo\_mux.prj

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\* Synthesis Options Summary \*

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---- Source Parameters

Input File Name : "thirtytwo\_mux.prj"

Input Format : mixed

Ignore Synthesis Constraint File : NO

---- Target Parameters

Output File Name : "thirtytwo\_mux"

Output Format : NGC

Target Device : xc3s200-5-pq208

---- Source Options

Top Module Name : thirtytwo\_mux

Automatic FSM Extraction : YES

FSM Encoding Algorithm : Auto

Safe Implementation : No

FSM Style : lut

RAM Extraction : Yes

RAM Style : Auto

ROM Extraction : Yes

Mux Style : Auto

Decoder Extraction : YES

Priority Encoder Extraction : YES

Shift Register Extraction : YES

Logical Shifter Extraction : YES

XOR Collapsing : YES

ROM Style : Auto

Mux Extraction : YES

Resource Sharing : YES

Asynchronous To Synchronous : NO

Multiplier Style : auto

Automatic Register Balancing : No

---- Target Options

Add IO Buffers : YES

Global Maximum Fanout : 500

Add Generic Clock Buffer(BUFG) : 8

Register Duplication : YES

Slice Packing : YES

Optimize Instantiated Primitives : NO

Use Clock Enable : Yes

Use Synchronous Set : Yes

Use Synchronous Reset : Yes

Pack IO Registers into IOBs : auto

Equivalent register Removal : YES

---- General Options

Optimization Goal : Speed

Optimization Effort : 1

Library Search Order : thirtytwo\_mux.lso

Keep Hierarchy : NO

Netlist Hierarchy : as\_optimized

RTL Output : Yes

Global Optimization : AllClockNets

Read Cores : YES

Write Timing Constraints : NO

Cross Clock Analysis : NO

Hierarchy Separator : /

Bus Delimiter : <>

Case Specifier : maintain

Slice Utilization Ratio : 100

BRAM Utilization Ratio : 100

Verilog 2001 : YES

Auto BRAM Packing : NO

Slice Utilization Ratio Delta : 5

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\* HDL Compilation \*

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Compiling verilog file "thirtytwo\_mux.v" in library work

Module <thirtytwo\_mux> compiled

No errors in compilation

Analysis of file <"thirtytwo\_mux.prj"> succeeded.

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\* Design Hierarchy Analysis \*

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Analyzing hierarchy for module <thirtytwo\_mux> in library <work>.

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\* HDL Analysis \*

=========================================================================

Analyzing top module <thirtytwo\_mux>.

Module <thirtytwo\_mux> is correct for synthesis.

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\* HDL Synthesis \*

=========================================================================

Performing bidirectional port resolution...

Synthesizing Unit <thirtytwo\_mux>.

Related source file is "thirtytwo\_mux.v".

Unit <thirtytwo\_mux> synthesized.

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HDL Synthesis Report

Found no macro

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\* Advanced HDL Synthesis \*

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Advanced HDL Synthesis Report

Found no macro

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\* Low Level Synthesis \*

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Optimizing unit <thirtytwo\_mux> ...

Mapping all equations...

Building and optimizing final netlist ...

Found area constraint ratio of 100 (+ 5) on block thirtytwo\_mux, actual ratio is 2.

Final Macro Processing ...

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Final Register Report

Found no macro

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\* Partition Report \*

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Partition Implementation Status

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No Partitions were found in this design.

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\* Final Report \*

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Final Results

RTL Top Level Output File Name : thirtytwo\_mux.ngr

Top Level Output File Name : thirtytwo\_mux

Output Format : NGC

Optimization Goal : Speed

Keep Hierarchy : NO

Design Statistics

# IOs : 162

Cell Usage :

# BELS : 96

# LUT3 : 64

# MUXF5 : 32

# IO Buffers : 162

# IBUF : 130

# OBUF : 32

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Device utilization summary:

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Selected Device : 3s200pq208-5

Number of Slices: 32 out of 1920 1%

Number of 4 input LUTs: 64 out of 3840 1%

Number of IOs: 162

Number of bonded IOBs: 162 out of 141 114% (\*)

[WARNING](WARNING:Xst:1336%20-%20%20(*)%20More%20than%20100%25%20of%20Device%20resources%20are%20used?&DataKey=SolutionRecord):Xst:1336 - (\*) More than 100% of Device resources are used

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Partition Resource Summary:

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No Partitions were found in this design.

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TIMING REPORT

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.

FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT

GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

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No clock signals found in this design

Asynchronous Control Signals Information:

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No asynchronous control signals found in this design

Timing Summary:

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Speed Grade: -5

Minimum period: No path found

Minimum input arrival time before clock: No path found

Maximum output required time after clock: No path found

Maximum combinational path delay: 9.124ns

Timing Detail:

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All values displayed in nanoseconds (ns)

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Timing constraint: Default path analysis

Total number of paths / destination ports: 224 / 32

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Delay: 9.124ns (Levels of Logic = 4)

Source: s0 (PAD)

Destination: Y<31> (PAD)

Data Path: s0 to Y<31>

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

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IBUF:I->O 64 0.715 2.026 s0\_IBUF (s0\_IBUF)

LUT3:I0->O 1 0.479 0.000 Y<9>\_F (N100)

MUXF5:I0->O 1 0.314 0.681 Y<9> (Y\_9\_OBUF)

OBUF:I->O 4.909 Y\_9\_OBUF (Y<9>)

----------------------------------------

Total 9.124ns (6.417ns logic, 2.707ns route)

(70.3% logic, 29.7% route)

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Total REAL time to Xst completion: 6.00 secs

Total CPU time to Xst completion: 6.17 secs

-->

Total memory usage is 186232 kilobytes

Number of errors : 0 ( 0 filtered)

Number of warnings : 1 ( 0 filtered)

Number of infos : 0 ( 0 filtered)